Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

1. (currently amended): A system for providing distributed dynamic functionality in an electronic environment comprising:

a plurality of platforms, the platforms suitable for providing a logic function, each of the platforms including an embedded programmable logic, a memory and a reconfigurable core, the logic, the memory and the reconfigurable core communicatively coupled via a fabric interconnect; and

a map expressing logic functions of the plurality of platforms,

wherein the platforms and the map are used for integrated circuit design.

2. (original): The system as described in claim 1, wherein the map includes instruction set architecture extensions and embedded programmable logic core adjuncts.

3. (original): The system as described in claim 1, wherein the map describes logic functions as provided by the plurality of platforms on a cycle-by-cycle basis.

4. (original): The system as described in claim 1, wherein the map describes logic functions as provided by the plurality of platforms in a manner so as to express groupings of platforms of the plurality of platforms utilized to perform the logic function.

5. (original): The system as described in claim 1, wherein the embedded programmable logic includes at least one of programmable gate arrays, sea of adders, CPLD structures and programmable circuit elements definable from a stored representation.

6. (original): The system as described in claim 1, wherein the fabric interconnect is isochronous.

7. (original): The system as described in claim 1, wherein the plurality of platforms is communicatively coupled via a fabric interconnect that is isochronous.

8. (original): The system as described in claim 1, wherein instruction set extensions are utilized through the use of the map to coordinate discrete instruction set extensions on a cycle-by-cycle basis and execution is synchronized across the plurality of platforms utilizing an isochronous fabric interconnect so that the instruction set extensions are utilized by corresponding platforms at a corresponding cycle.

9. (currently amended): A method for providing an executable suitable for being employed by a plurality of platforms, comprising:

receiving a program of instructions;

determining availability of ~~a~~ the plurality of platforms for performing the program of instructions, each of the plurality of platforms including an embedded programmable logic, a memory and a reconfigurable core, the logic, the memory and the reconfigurable core communicatively coupled via a fabric interconnect that is isochronous, wherein availability of the platforms includes at least one of load value of the platforms and functionality of the platforms; and

translating the program of instructions into an executable suitable for operation by the plurality of platforms based on the determined availability,

wherein the plurality of platforms are used for integrated circuit design.

10. (original): The method as described in claim 9, wherein availability of the platforms is determined by referencing a map.

11. (original): The method as described in claim 10, wherein the map expresses logic functions of the plurality of platforms.

12. (original): The method as described in claim 10, wherein the map includes instruction set architecture extensions and embedded programmable logic core adjuncts.

13. (original): The method as described in claim 10, wherein the map describes logic functions as provided by the plurality of platforms on a cycle-by-cycle basis.

14. (original): The method as described in claim 10, wherein the map describes logic functions as provided by the plurality of platforms in a manner so as to express groupings of platforms of the plurality of platforms utilized to perform the logic function.

15. (currently amended): A system for providing distributed dynamic functionality in an electronic environment comprising:

a plurality of platforms communicatively coupled via an isochronous fabric, each of the platforms suitable for providing a logic function, the platforms including an embedded programmable logic, a memory and a reconfigurable core communicatively coupled; and

a map expressing availability of the plurality of platforms for performing a logic function

wherein the platforms and the map are used for integrated circuit design.

16. (original): The system as described in claim 15, wherein the map includes instruction set architecture extensions and embedded programmable logic core adjuncts.

17. (original): The system as described in claim 15, wherein the map describes logic functions as provided by the plurality of platforms on a cycle-by-cycle basis.

18. (original): The system as described in claim 15, wherein the map describes logic functions as provided by the plurality of platforms in a manner so as to express groupings of platforms of the plurality of platforms utilized to perform the logic function.

19. (original): The system as described in claim 15, wherein the embedded programmable logic includes at least one of programmable gate arrays, sea of adders, CPLD structures and programmable circuit elements definable from a stored representation.

20. (original): The system as described in claim 15, wherein the fabric interconnect is isochronous.

21. (original): The system as described in claim 15, wherein instruction set extensions are utilized through the use of the map to coordinate discrete instruction set extensions on a cycle-by-cycle basis and execution is synchronized across the plurality of platforms utilizing an isochronous fabric interconnect so that the instruction set extensions are utilized by corresponding platforms at a corresponding cycle.

22. (currently amended): A system for providing distributed dynamic functionality in an electronic environment comprising:

a plurality of platforms communicatively coupled via an isochronous fabric, each of the platforms suitable for providing a logic function, the platforms including an embedded programmable logic, a memory and a reconfigurable core communicatively coupled; and

a means for providing a map expressing availability of the plurality of platforms for performing a logic function,

wherein the platforms and the map are used for integrated circuit design.

23. (original): The system as described in claim 22, wherein the map means includes instruction set architecture extensions and embedded programmable logic core adjuncts.

24. (original): The system as described in claim 22, wherein the map means describes logic functions as provided by the plurality of platforms on a cycle-by-cycle basis.

25. (original): The system as described in claim 22, wherein the map means describes logic functions as provided by the plurality of platforms in a manner so as to express groupings of platforms of the plurality of platforms utilized to perform the logic function.